Ceramic capacitors – how they are made, how they perform and where you should use them – by Cyril Bateman.

Understanding CAPACITORS

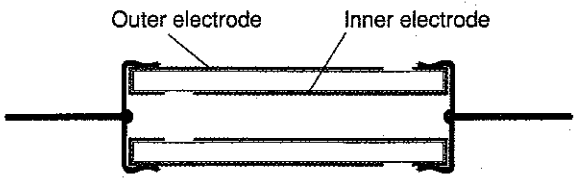
Ceramic capacitors possess two significant features not present in any other capacitor type. These are the ability to control the dielectric's temperature coefficient and its dielectric constant, K.

Variation of the dielectric formulation used can provide either the widest possible range of dielectric constants – and hence capacitance-to-size ratio – or alternatively the widest possible range of controlled temperature coefficients.

As with domestic pottery, these dielectric formulations can be used to produce an unlimited variety of sizes and shapes. When valves dominated electronic design, many obtusely-shape, and sometimes very large, capacitors were produced by first casting a basic shape and then machining it to size, prior to firing. Such custom designs are now very rare.

This unique ability to tailor dielectric formulations provides almost any desired temperature coefficient of capacitance, from minus 5600 to plus 100 parts per degree centigrade. Alternatively, dielectric tailoring can provide an extremely high K constant, up to 12000, giving increased capacitance. Both features resulted in the ceramic capacitors strategic importance in WWII valve operated equipments. Initially based on a tubular construction, the first ceramic capacitors were assembled using production techniques derived from established resistor manufacturing methods.

Fig. 1. Cross section of an axial leaded tubular ceramic capacitor looks and behaves exactly like a co-axial transmission line. Depending on the physical dimensions and its dielectric constant K, it can have a very low characteristic impedance. Its electrical length may be 50 - 100 times greater than its physical length, when made with high 'K' ceramic.



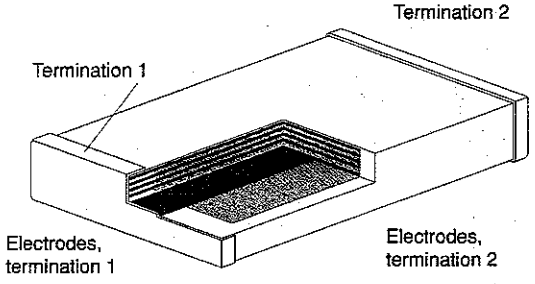


Fig. 2. Sectional view of a typical multilayer chip capacitor, clearly showing how alternate electrode layers connect in turn to each termination. Using high-K ceramic and thin dielectric layers, for maximum capacitance possible in a small size chip.

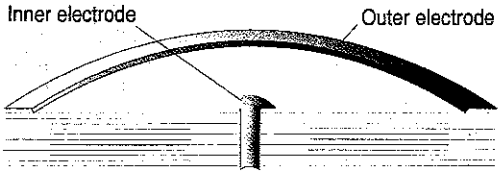


Fig. 3. Developed from the basic multilayer, this discoidal construction provides high capacitance in a small size. The lead-through centre hole and multiple grounded electrodes ensure electrical screening from top to bottom faces.

The Erie company implemented volume production of ceramics at its Pennsylvania plant shortly before WW2. Subsequently, production commenced at Erie Resistor Ltd, the company's UK subsidiary.

Using Type1 dielectric, capacitance as low as 0.5pF was possible, and with high-K dielectric up to 10nF. Both of these values could be produced with a 500V working rating. Uniquely, this tubular construction could be automatically 'silvered' to value, permitting very close tolerances, **Fig. 1.**

The disc alternative

This tubular capacitor format remained dominant until the pressed disc capacitor was developed some years later. Designed for increased volume and reduced costs, this construction resulted in a capacitor then costing little over one old pence. Capacitances from 0.5pF up to 10nF and 500V working in a 9mm diameter disc size were produced.

By pressing thicker discs, much higher voltages could be supported – even up to 30kV. Increased disc diameter up to 31mm, substantially increased the capacitance attained at any

tage. The larger disc capacitor makers were able to select from as many as fifty production-proven dielectric formulations.

Increasing use of transistors for portable radios demanded lower-cost, higher-capacitance and lower voltage disc ceramics. To cater for these needs, the so-called *Transcap* or barrier-layer capacitor was developed. On a 15mm disc, this construction could provide 0.22µF at 10V.

The sixties saw the development of the first solid-state computer, the IBM *360*, which was used for the MinuteMan missile. It required even larger capacitances in even smaller sizes – and high reliability. The recently invented multilayer[1] ceramic capacitor was seen as the ideal solution. Initially only produced in the USA, the multilayer capacitor soon became established in the UK. By 1964, volume production of UK manufactured multilayer capacitors, was established at the Erie UK factory.

Subsequent developments in the multilayer capacitor's construction and manufacturing process ensured its world-wide domination[2]. Ii was initially produced as a leaded product, dipped in encapsulating resin for commercial use, or transfer moulded for more demanding environments.

..apacitors without leads

In 1969, the basic multilayer component 'chip' was marketed without lead wires or finish, for use in the production of the new thick-film hybrid assemblies. Developments in the termination metals to prevent solder leaching and in the construction to reduce the effects of thermal shock resulted in the first generally used surface mounting capacitor, **Fig. 2**.

The military missile and NASA Apollo programmes of the late sixties demanded smaller, lighter, very-high-frequency capable, emc filters. For both requirements, these filters had to survive extremely high 'G' forces and vibration conditions, as well as temperature extremes.

To suit these needs, a special multilayer device called the discoidal capacitor was developed. It comprised a circular multilayer chip with one termination at its central lead-through hole and the other formed by the disc's periphery.

This discoidal construction provided three unique benefits. Electromagnetic signal currents presented at the 'hot' centre hole, rapidly dispersed into the 360° electrode system. Since connections extended all round the circumference, providing an almost zero inductance ground path, the discoidal provided high attenuation at the highest frequencies.

Soldered into a tubular metal casing, these grounded electrodes provided almost perfect high-frequency isolation between the 'dirty' input and the 'clean' output sides. Today this discoidal construction remains dominant for high-frequency lead-through emc filters and similar applications. It is used whenever screening between a dirty input and clean output is needed, **Fig. 3**.

Planar array ceramics

Developed from these early discoidal concepts, the latest multilayer capacitors include multiple-lead-through emc filter capacitors known as planar arrays. These are produced with mechanical dimensions compatible with commercial and military connectors, or as a custom ordered part having almost any desired shape or size.

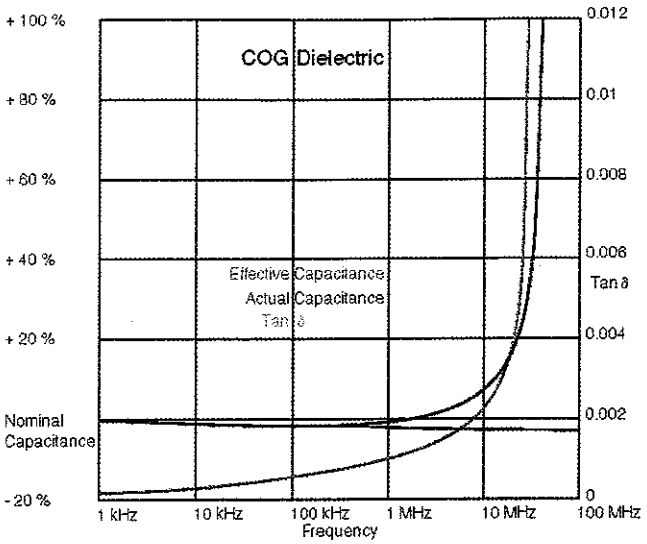


Fig. 4. Since the K of COG dielectric is almost constant with frequency, the sharp increase in measured or effective capacitance, also tan δ as resonance approaches, can be seen. This increase results from the combined reactances of the actual capacitance and the capacitor's self-inductance.

While covering the main stream ceramic products, this brief overview deliberately skips over many styles that were important at their time but that are now redundant. These include the lead-less disc, the wedge capacitor, the very-thin single-layer 'Weecon', the colour-television tripler/quadrupler capacitor, the very-large and thick extra high voltage cupped capacitor, and the wound or 'rolled' tubular multilayer ceramic. The wedge capacitor was common in early vhf amplifier and tuner assemblies while the wound tubular multilayer design was popular in the early sixties in USA for use in emc filters.

Shocking soldering

In the seventies, as more sophisticated or leadless ceramic capacitors became generally used, thermal shock during soldering was a major discussion topic and the cause of most early capacitor failures.

At that time, a second serious soldering problem using conventional methods was that the terminations of these non-leaded parts 'leached' away. Unless the soldering time and temperature were minimised, the precious metal termination would simply dissolve into the molten solder, resulting in a visible capacitor failure. Unfortunately, steps taken to minimise thermal shock often aggravated the leaching problem.

Following significant improvements in termination materials and electroplating, the amount of time that the solder can remain liquid has increased ten-fold. Electrode and termination leaching has been eliminated and most capacitor makers now publish clear soldering guidelines.

Thermal shock creates minute cracks within the ceramic

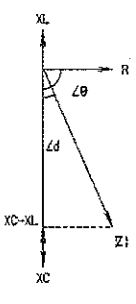


Fig. 5. This vector diagram shows the relationship between tan δ and cos θ. Both are essentially equal at small loss angles. The interaction between the capacitance X_C and self inductance X_L vectors, which causes series resonance, is also visible.

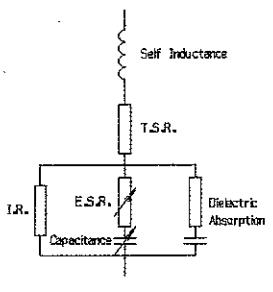


Fig. 6. This equivalent circuit for a practical capacitor is valid for all frequencies up to self resonance and perhaps one octave higher. When mounted onto a microstrip line, an additional small capacitance, not shown, between the capacitor mounting points to earth will also be present.

dielectric, generally close to its interface with the end termination materials. Initially these cracks might be small, and the capacitor will appear undamaged. But with time, operating temperature fluctuations and mechanical stress due to printed board flexure, these cracks grow. Ultimately the capacitor fails, usually as a short circuit.

You might question why ceramic capacitors are so prone to this damage. After all common household ceramics or pottery seem able to survive considerable temperature stress.

Self inductance

Some readers have queried my description[9] that physical size equates to self inductance.

The self inductance of a single straight wire or a track on a printed circuit board can me measured and calculated. Similarly, self inductance for a ceramic chip capacitor can also be estimated, given the capacitor's electrode shape and size. However this self inductance can more easily be measured.

Measurements of the K value by frequency of a test block of dielectric in a dielectric test jig[12] confirms that COG types have a K value almost constant, reducing only slightly with frequency. But high-K materials exhibit a substantial reduction.

Consequently, using COG dielectric, the observed series resonance frequency together with the 1MHz capacitance value can be used to determine the capacitor's self inductance with acceptable accuracy, **Fig. 4**.

Conventional measurements of impedance magnitude – usually published in makers data in logarithmic format – show impedance reducing with frequency to a sharp minimum at resonance, then increasing with further frequency increase. Since most designers prefer to use capacitors below the series resonance, published plots usually stop soon after this resonance has been shown.

Measurement of the chip capacitor's impedance as a vector of resistance (esr) and reactance (jX) initially follow exactly this same pattern. But at this series resonance frequency, they clearly show reactance crossing the zero line – a change from negative to positive phase angles with increase of frequency, **Fig. 7**.

For these measurements to be valid, it is essential to eliminate all test jig parasitics, both capacitance and inductance, by applying open, short and load calibration of a vector network analyser. This must be done at each measurement frequency, and at the precise point in a transmission line where the test capacitor will be mounted. Next, 12-term, also called 'full 2 port' error corrections must be applied.[8]

When it is not feasible to apply the open, short load, calibration as above, calibrate at the ends of the test coax cables, which attach the test jig and apply 12 term correction. Characterise the test jig by measuring it with an open, short and known impedance, in place of the test capacitor, at each frequency of interest. These measured error values are then applied using established equations as a means of error reduction. Remember though that each of the measurement and error terms described by the correction equations are vectors or complex numbers and must be calculated accordingly.[13] For open short and load,

$$Z_{dut} = \frac{Z_{standard.true}(Z_{jig.open} - Z_{standard.measured})(Z_{dut.measured} - Z_{jig.short})}{(Z_{standard.measured} - Z_{jig.short})(Z_{jig.open} - Z_{dut.measured})}$$

While I plan to detail to these capacitor measurement techniques in a later article, to demonstrate this self inductance, I took four capacitors, previously characterised up to 1MHz. Using an HP4815 vector impedance meter, I measured all four capacitors at frequencies from 1MHz to 100MHz, and applied the 'open/short/load' error-correction algorithm shown to the measured values, **Fig. 7-10**.

To simplify the calculation and plotting of these results – which involved many complex numbers – I stored the measured jig correction values by frequency in a database and used my custom written, dedicated 'open/short/load' error correction calculation and plotting software.

From this resonant frequency and the inductive reactance with increasing frequency, the capacitor's self inductance can be calculated.

The capacitor ceramic formulations used are quite different, comprising in most cases a mixture of many materials. While the high K formulations may be based on barium titanate, small quantities of many oxide or rare earth additives, together with 'frits' or glasses will be used.

During firing, or sintering, the dielectric is raised in a controlled manner to very high temperatures. Firing temperatures are deliberately chosen to avoid notable melting or alloying of these constituents, or any significant crystal growth.

A multilayer capacitor is essentially a multitiered sandwich of alternating layers of thin ceramic dielectric and precious metal electrodes. The whole laminate of metal and ceramic is co-fired together, the electrode metals must not oxidise or melt at the firing temperatures needed. As a result, precious metals are used.

Dielectric ceramic and the precious metals used have quite different expansion coefficients and thermal conductivity. Temperature differences within the capacitor can result in mechanical stress due to differential expansions, both within the basic ceramic materials and at the ceramic metal interfaces.

Development of sintering methods, dielectric formulations, electrode and termination materials, have produced dramatic improvements, resulting in today's ceramic chip capacitor found on almost every surface-mount circuit board.

But even with today's much improved products and production methods, a degree of thermal shock hazard remains. Since the capacitor ceramic is extremely hard, brittle and easily chipped, the most common problem results from mechanical cracking. This is induced by poorly adjusted assembly and board testing equipment. Each surface mounting ceramic chip capacitor maker provides handling, soldering and mounting recommendations that must be observed.

How is the dielectric made?

So just how are these ceramic dielectrics manufactured?

All ceramic and precious metal-electrode ink formulations are closely guarded, proprietary secrets. In addition, these formulations, and the capacitor processing methods used, are intimately interdependent and so I can only discuss them in broad outline.

With many dielectric formulations, minute percentages of additives and dopants are be used. Consequently, levels of impurities in each ingredient are important.

Having satisfied conventional chemical and physical analysis, each new delivery of a material is used to make a batch of test capacitors. Performance of these capacitors is verified against the test specifications, including microscope examination of capacitor sections.

Each ingredient is weighed out, added to a solvent and placed into a rotating 'ball' mill, together with the correct weight and sized balls of flint or borundum.. The mill is rotated for many hours, even days, to blend together all ingredients and achieve any needed ceramic particle size reduction.

Having removed the grinding balls, these ingredients, now finely dispersed and suspended in the solvent, are injected as a fine dry powder, needing only analysis to confirm correct particle size. The tower needed to dry a typical 50kg charge of powder may be as tall as 20ft.

Traditional ceramic capacitors

The powder can be used to make capacitor dielectric in several ways. For tubular capacitors it is mixed with solvent and plasticiser and machine kneaded to an air-free, stiff, dough-like consistency. This dough can be pressure extruded, like toothpaste, to the desired tubular dimensions. Dried and cut to length, it is ready for firing.

For disc capacitors, the powder is used dry, being fed into

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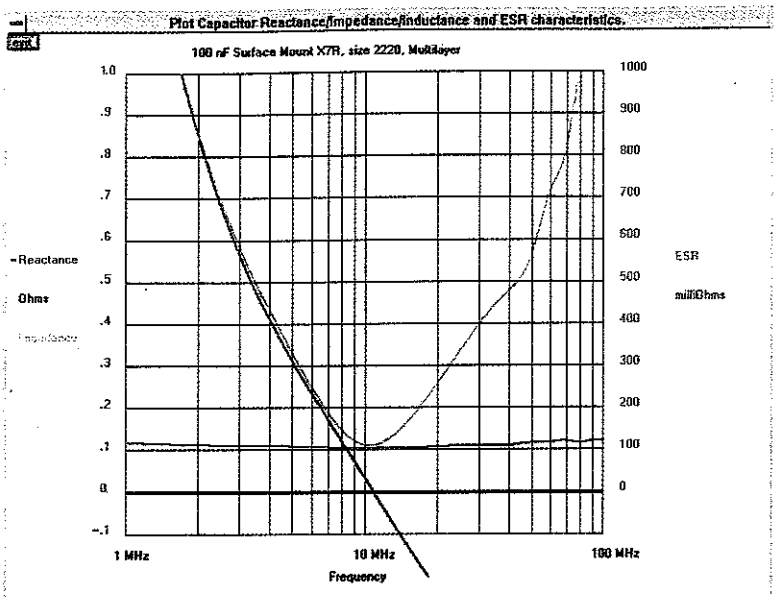

Fig. 7. This specially produced plot of measured reactance, impedance and esr of a typical 100nF X7R chip, shows reactance changing from negative to positive, at resonance. The impedance plot increases above resonance as expected, from a minimum value, equal to the measured equivalent series resistance. For clarity only, the reactance scale has been inverted, having negative values in the upper plot.

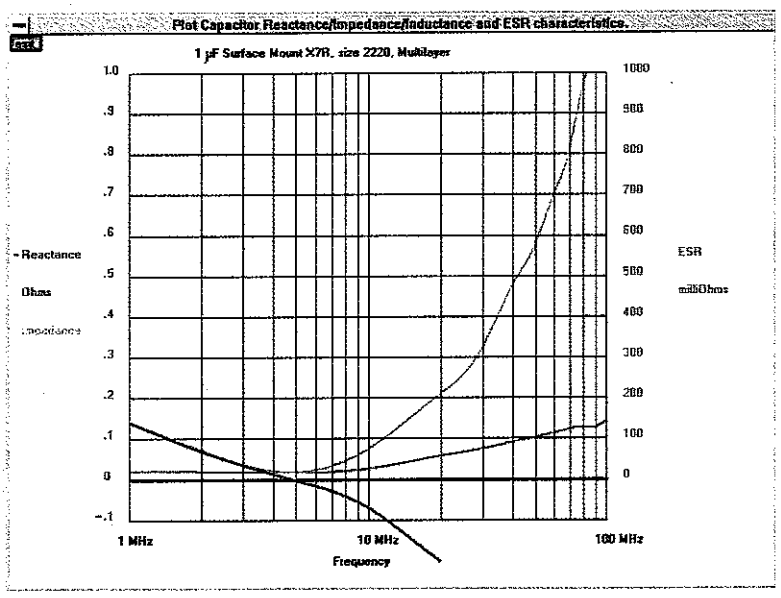

Fig. 8. Similar to Fig. 7 – same size chip and typical 1µF X7R capacitor. As expected the resonance frequency has reduced, but otherwise all curves follow the same trends.

tungsten carbide press tools and subjected to very high pressure presses. High volume production discs can be pressed using multi-station, high speed, single action rotary turret presses, similar to those used to make medicinal pills. Larger discs and pressed tubes however need double-action presses, usually single station, equipped with both top and bottom acting press tools.

Multilayer ceramic capacitors

Early multilayer capacitors were made using the 'dry film' method.[1] The required thin dielectric film was produced by passing a plastic film carrier through a plasticised ceramic 'slip' at controlled speed, to emerge coated with ceramic. After drying, this heavily plasticised ceramic could be stripped off as a thin, self supporting, flexible ceramic film.

To produce the alternating electrode patterns needed for a multi-layer device, the ceramic was screen printed with electrode ink. The dry electroded ceramic film was stacked, layer on layer, to produce a 'stick' of capacitors. Compacted under high pressure, these sticks were then diced into individual capacitor chips, ready for firing.

Later developments allowed similarly thin ceramic films to be continuously cast onto a moving polished stainless-steel belt. This eliminated the plastic carrier film and needed smaller amounts of plasticiser.

The reduction of plasticiser content is important. While, as with domestic pottery, all ceramic shrinks during firing, shrinkage increases with increased quantities of plasticiser and organic binders.

Introduced in the early eighties, the modern 'wet-film' method[3] involves screen printing, in turn, unplasticised ceramic and a matrix of electrode ink patterns. These are precision printed on to a dimensionally stable carrier.

After hot-air drying, the carrier is returned to the printer head and further layers of ceramic or electrode patterns are added until the capacitor is complete. Following final drying, these sticks of capacitors are separated into individual capacitor chips, ready for firing.

With either assembly method, the electrode inks used depend on the ceramic formulations and their firing temperature. For lower firing temperatures, a combination of palladium with silver is often used. At higher firing temperatures, the silver would melt and globulate, so it must be replaced by more costly gold or platinum, depending on the temperature.

Firing the ceramic

Two main methods of firing the ceramics are used. Traditional ceramic capacitors produced in large volumes are often fired in long, temperature controlled multi-zone, continuously operated 'sagger push' kilns.

The pusher kiln is built using high-density refractory bricks and can take days to bring up to temperature and stabilise. More modern, smaller and lighter batch kilns are quite different. Built using extremely low density refractory linings, they allow firing cycles with pre-set individual time and temperature profiles.

As with conventional household pottery, the fired ceramic shrinks significantly from its unfired or 'green' size. While principally dependant on the amounts of organic binders and plasticisers used in the ceramic formulation, change of the firing profile also affects shrinkage.

Organic materials and plasticisers in the raw ceramic have to be removed by a slow pre-fire before the final firing. A complete firing cycle may take as long as two or three days.

The 'wet film' multilayer and the pressed disc processes use the least quantities of organic and plasticiser so shrink least of all. Shrinkage is especially important where a precise finished size ceramic is needed, as for the planar array, multi-hole, capacitor designs.

For both kiln types, very precise control of temperature and the time/temperature profile is essential, to standardise ceramic shrinkage and optimise capacitor yield.

Adding a means of connection

The fired multilayer ceramic capacitor needs only the application of external precious metal ink terminations, to contact the electrodes to produce a capacitor chip.

Disc or tubular ceramics first have to have their precious metal electrodes applied. This is usually silver ink. The external terminations and the silver electrodes are fired for a much shorter time and at lower temperatures than the ceramic.

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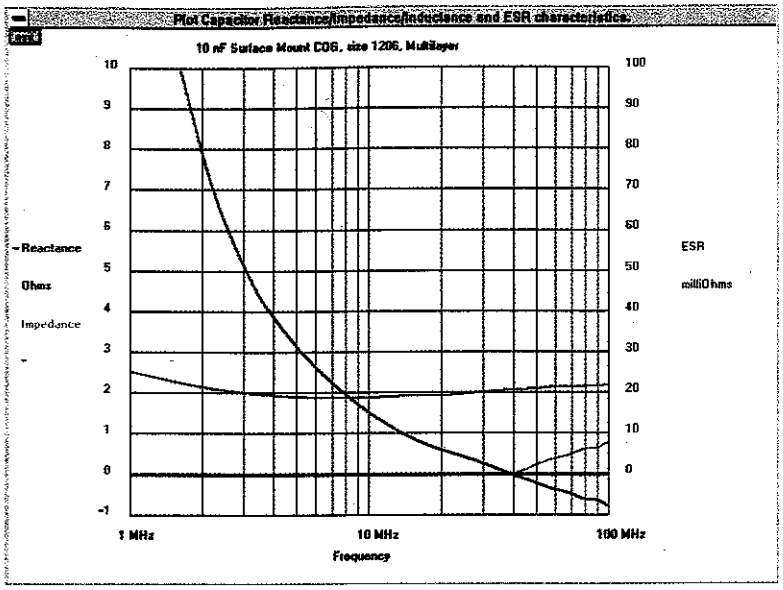

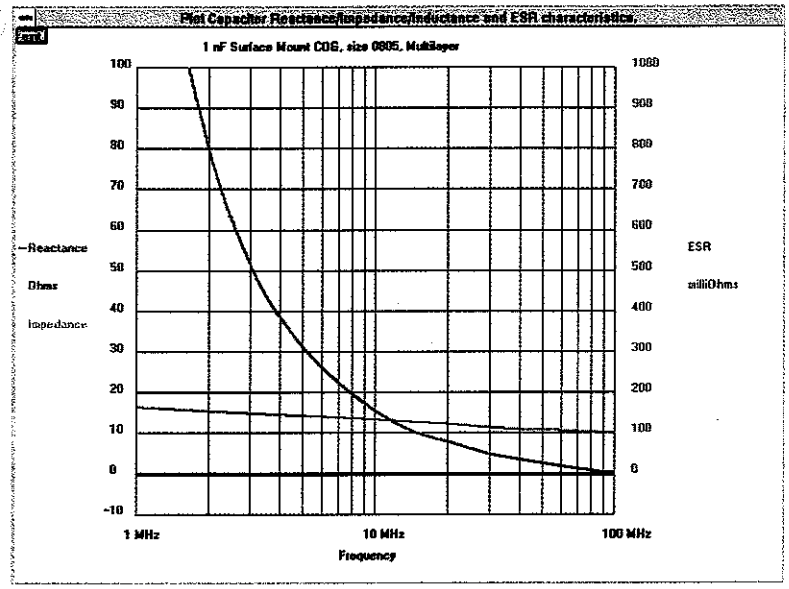

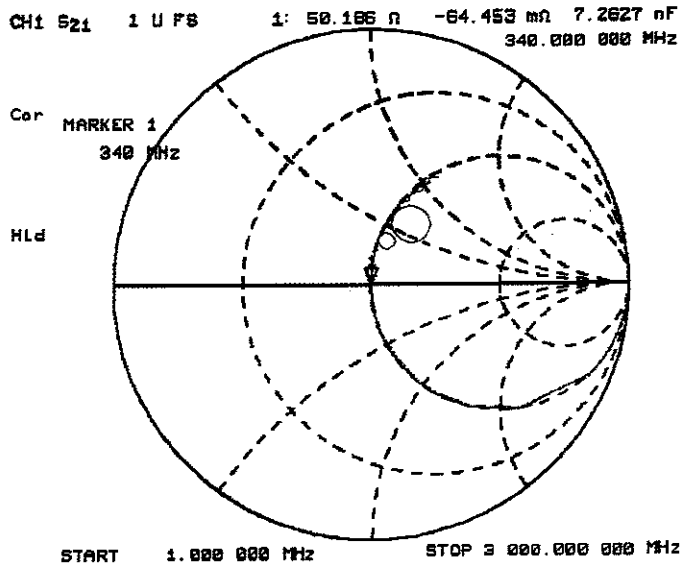

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Top: Fig. 9. This plot of a 1206 sized 10nF COG chip shows a much higher resonant frequency, resulting from its smaller physical size, hence less self inductance, and its reduced capacitance.

Middle: Fig. 10. A similar plot of a 1nF COG chip shows resonant frequency exceeds the 100MHz measured. This plot was deliberately taken to demonstrate the effectiveness of the error correction method. Maker's data suggests resonance should be 150MHz. Uncorrected resonance, due to jig parasitics, was measured at 56MHz.

Bottom: Fig. 11. This Smith chart S21 impedance plot of a 300pF chip mounted as 'shunt' to ground, on a 50Ω microstrip line jig, shows the trace changing sign at series resonance. Above this series resonance frequency, other resonances can be seen which remain in the upper inductive half of the chart. The low frequency straight sections result from values changing rapidly between measured frequency points. Courtesy Syfer Technology.

The barrier layer or Transcap capacitor differs in that the basic ceramic discs are fired twice. Following the conventional oxidising firing in air, these capacitors undergo a second firing in a reducing atmosphere. This renders the ceramic material conductive, with only a few ohms resistance.

Once the termination silver has been fired in air, two capacitors, one on each face, are formed about the conducting central core. Their dielectric is extremely thin. This reduces the working voltage, but increases the capacitance tenfold.

After termination or electrode firing, the capacitor is ready for any final assembly processes. Lead wires can be attached and the capacitor encapsulated. Surface-mount chip capacitors may have their end terminations hot solder coated, electrotinned, nickel plated or silver-palladium coated depending on the application they are intended for.

In manufacture, all heat process stages are strictly profiled and controlled. To ensure this, each stage of production may be subject to statistical process control analysis of yields.

All soldering operations use a controlled pre-heating stage. Terminations or electrodes incorporating fired silver-bearing inks are soldered using an alloy pre-saturated with silver to minimise leaching. One such alloy is LMP or SN62. This product is tin, lead and silver in the proportions of 62/36/2. It is a true eutectic, i.e turns immediately from solid to liquid, which minimises the possibility of dry joints.

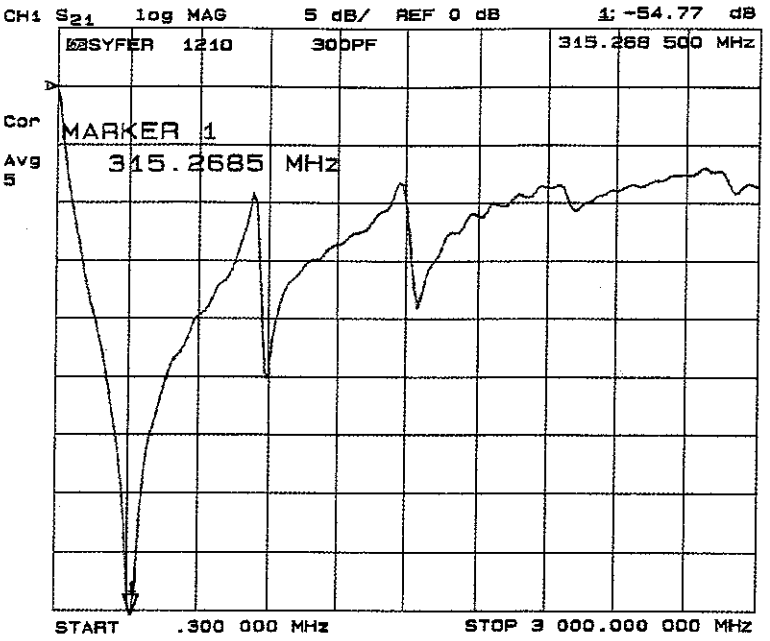
Other metals can dissolve or leach into molten solder so the choice of solder alloy is important. If fine copper wires need tinning, for example, copper loaded solder is a good choice.

Dielectric characteristics

EIA Class I, ultra stable, COG. For almost all circuit needs, the conventional COG ceramic provides the nearest perfect capacitor, having better characteristics than mica or any film type, except perhaps for PTFE. It has a temperature coefficient of ±30ppm, negligible voltage coefficient, capacitance stable over time, negligible capacitance variation at high frequencies, minimal dielectric absorption and a 'Q' approaching 1000 at 1MHz, **Fig. 4**.

A capacitor's effective or measured capacitance rises sharply at series resonance. This is the effect of the positive and increasing reactance of its self inductance, approaching then exceeding that of the negative and reducing reactance of the actual or true capacitance at the resonant frequency.

Apart from the steady decline in K which most dielectrics exhibit with frequency increase, the K value of the dielectric is unchanged at resonance, **Fig. 5**. The panel on capacitor self inductance provides more on this topic.



op: Fig. 12. This rectangular plot of Figure 11 clearly shows multiple high-frequency harmonic resonances occurring, having smaller amplitude nulls than that of the series resonance. These amplitudes reduce with frequency, as capacitor losses increase. Courtesy Syfer Technology.

Middle: Fig. 13 Schematic section of the Hewlett Packard 16091A, low cost coaxial test jig. Each capacitor chip being pre-soldered to two contact pins. The 1mm displacement between calibration and measurement planes can be mathematically corrected, eliminating all jig parasitics.

Bottom: Fig. 14. Plot of an actual measurement of a COG 600pF 1210 chip using the Hewlett Packard 16091A coaxial test jig. The capacitor is shown as an inductance of 1.8275nH while at a higher frequency resonance. Its series resonance is at 185MHz. For ease of calculating corrections, this admittance plot is preferred to the more common impedance presentation. Courtesy Syfer Technology.

Since the surface-mounted ceramic multilayer COG chip provides a large capacitance in a small size, together with low self inductance at low cost, it is invaluable for high frequency circuits. At the high end of the rf spectrum, especially when stripline circuits are involved, an improved high-Q version[3,4,5] is also available. For low capacitance values, this device can offer a Q of around 1000 at 100MHz.

There are two further types of capacitor that maintain these high Qs to even higher frequencies, albeit at higher cost. These are the ACCU-F[6] – a thin-film capacitor made using silicon dioxide and silicon nitride – and the porcelain multilayer chip[7] capacitor.

Using the best available *LCR* meters at 1MHz, differences in Q between these styles cannot be measured with certainty. Such performance differences can only be measured at higher frequencies, using the best possible jig techniques, together with a 12 term error corrected vector network analyser.[8]

High-K dielectrics

Higher capacitance values are available using high-K X7R, Y5V and Z5U dielectrics. These materials provide the best capacitance, voltage and size combination of all, by trading off temperature coefficient, capacitance loss with frequency and voltage coefficient.

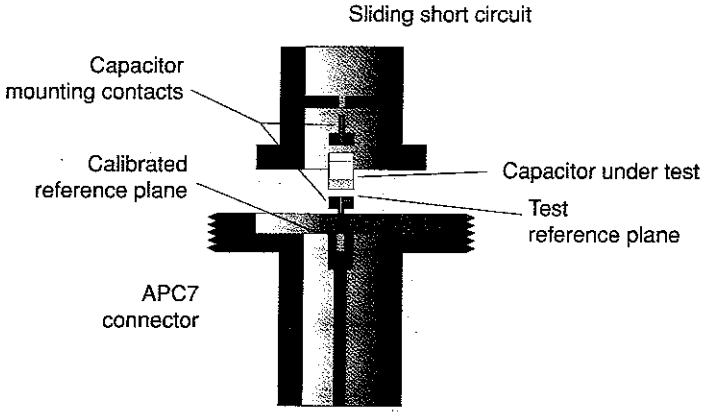
The stable X7R, EIA Class II and the general purpose Z5U/Y5V, EIA Class III grades, are controlled according to windows of temperature coefficient. While each maker's capacitors will comply with these windows, different makers' temperature coefficient curves may follow quite different contours. These high-K capacitors exhibit change of capacitance with voltage, frequency and temperature.

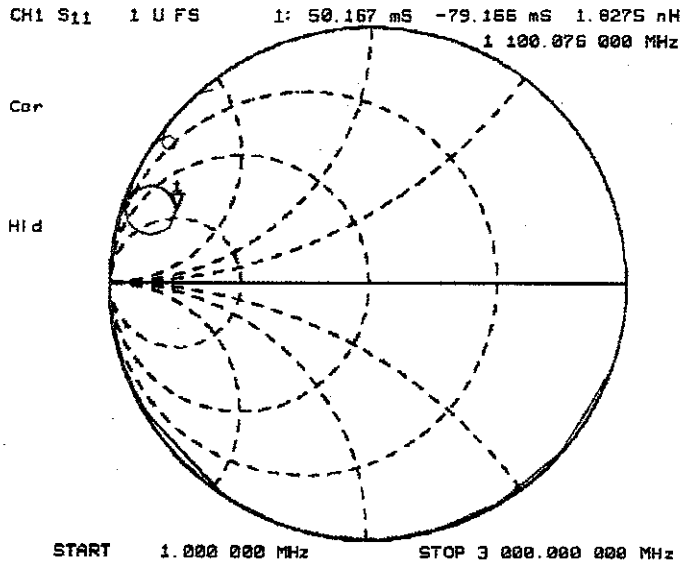
Based on barium-titanate, which is a polar material, high-K capacitors also exhibit a modest level of charge retention. This is called dielectric absorption, and I hope to explore this topic in a future article[9].

The crystalline structure of ceramics based on barium-titanate changes on being heated above the Curie point, which is notionally 125°C. On cooling, this domain structure relaxes with time, reducing the K value in a logarithmic manner. It effectively becomes stable after 1000 hours. As a result, capacitors made using these dielectrics are manufactured to age down to nominal capacitance, having rested or aged for 1000 hours following their last heat cycle.

Any subsequent soldering process that takes the dielectric over 125°C restarts this ageing cycle. Full details of the ageing factors to be applied will be found in makers' data sheets.

Capacitors based on high-K ceramics provide the best possible capacitance versus volume performance while maintaining stability within defined limits. The small physical lengths permitted ensure very low self inductance, extending





the upper limits of the high-K capacitor's frequency range.

You may wonder just why a low self inductance value matters. At some frequency, the reactance of this self inductance becomes equal in value to that of the capacitor's reactance. But since the two reactances are opposite in phase, a series-

resonance effect results.

At higher frequencies, while still blocking dc, the capacitor otherwise behaves as though it were an inductor, thus limiting its upper usable frequency for most circuits.

As the clock frequency of logic chips becomes ever higher, the decoupling of switching spikes becomes increasingly difficult. Any self inductance in the decoupling capacitor slows or impedes the rate at which the capacitor is able to charge or discharge in order to decouple these spikes.

An easy way to lower a capacitor's self inductance is to reduce its physical length or increase its width. But reducing the inductance further is only possible using specially designed capacitors. One company particularly active in reducing capacitor self inductance, AVX, offers several application notes via its Web page and on cd-rom.[10]

Allowing for all these variants, a capacitor's behaviour at

Measurements at rf

While the 100MHz measurements suffice for general applications, for rf design they are little better than dc measurements. While specialist capacitor measuring equipment is available[14,15] to measure up to 1 and 1.8GHz, it is very expensive and not available in many laboratories.

Two suitable instruments more commonly available are the *HP8510,* which measures from 45MHz to 110GHz, and the *HP8753* which measures from 300kHz to 6GHz. I have used each of these vector network analysers. Both have 12-term error correction.

The Smith-chart presentation provided by these analysers is particularly relevant when demonstrating the self inductance of a capacitor. It displays the measured impedances by frequency, in terms of $R+-jX$, where $jX=j(X_C-X_l)$.

When jX has a negative net value, i.e. a capacitive reactance, it will be plotted below the horizontal centre line. When jX has a positive net value, or an inductive reactance, it is plotted above the centre line. When jX is zero, i.e. resistive, it is plotted along the central horizontal line.

On this impedance chart, the right-most limit of the central line represents infinity while the left most limit represents a short circuit. Consequently, when measuring a capacitor, the frequency at which the trace crosses the central line represents the capacitor's self resonant frequency.

In the example shown, this occurred slightly below 340MHz. The small circular loops, or whirls, represent a resonant behaviour, but since the trace remains above the centre line, the capacitor has continued to present an inductive reactance, **Fig. 11**.

Obviously, the highest frequencies pose considerable problems when it comes to designing and characterising test jigs. While commercial jigs are available from Wiltron[16] and Hewlett Packard[17], they are extremely expensive. However up to perhaps 3GHz, and ignoring phase, relatively simple jigging can be used to measure resonance, and hence self inductance of low value capacitors. The same jigging can be used to observe transmission line behaviour.

S_{21} measurements. For magnitude parameters only, the easiest method is to measure the chip's insertion loss when mounted as a shunt to earth in a good 50Ω microstrip line. While for a quick look-see FR4 board could be used, its characteristics change dramatically with frequency, making it impossible to produce a good wideband 50Ω line.

For these measurements, I fabricated accurate lines using Rogers *Duroid 5880* PTFE board[18], gold plated, with *APC3.5* surface launching connectors.

You may question why this insistence on using a good 50Ω line. Almost all modern measuring systems have a 50Ω input and output impedance, as does suitable quality connecting cables. Using a jig of impedance other than 50Ω produces a reflection of power at the point where the jig is connected to the 50Ω system. This reflected power reduces that incident on the test capacitor, giving misleading results.

For insertion loss, or S_{21}, measurements this jig mismatch also causes reflections, hence ripples in the receiver measurements. Unless the vector network analyser used has capability for 'Thru/Reflect/Line' jig calibration,[19] these errors cannot be removed. As a result, they must be avoided when designing and characterising any test jig.

The rectangular plot of S_{21} insertion loss of a capacitor in a 50Ω microstrip line, mounted from line to ground, clearly shows the capacitor self resonant at 315.2685MHz. A second, parallel resonance, resulting from stray capacitances with the chip self inductance might also be expected at a very much higher frequency.

Other resonances are clearly visible, but since the net reactance shown in the Smith plot remains inductive, these cannot result from either series or parallel circuits. These resonances exactly mimic those seen when measuring low impedance, high capacitance transmission lines that are grossly mismatched. As frequency increases, the chip's losses increase, reducing the amplitudes of the higher frequency resonances, **Fig. 12**.

S_{11} measurements. While the above measurements can characterise all four possible S-parameter characteristics, S_{11}, S_{21}, S_{12} and S_{22}, of the capacitor in a two port system by frequency, an alternative single-port characterisation of S_{11} only is also possible. This measurement can determine resonant frequencies, capacitor self inductance, equivalent series resistance and capacitance by frequency.

One special benefit of measuring only S11 is that a commercial test jig is available for smaller chip capacitors, at a reasonable cost. The *HP16091A* jig requires the chip to be soldered to two contact header pins, which permit the capacitor to be inserted into the central conductor of either a 7mm or 10mm variable length coaxial airline.

The point of connection of this jig to the measuring system can be fully calibrated using *APC7* open, short and load impedance standards, **Fig. 13**.

The header pins displace the test capacitor by some 1mm from the calibrated reference plane and introduce parasitics of resistance, inductance and capacitance. In the measurement shown, this test jig was used, so the on-screen display as plotted, includes jig parasitics.

Similar looping but inductive resonances are clearly visible and the self inductance of the jig mounted capacitor, is shown as 1.8275nH. While the Smith chart default is to display impedance, the S_{11} plot of admittance values shown, facilitates calculation of the error corrected results, **Fig. 14**.

Using suitable open and short-circuit dummy capacitors, these test jig strays can be separately quantified and used for error reductions using a computer. This results in an accurate measurement of S_{11}, for the capacitor being tested.[20]

$$R_x = \frac{G_m - G_o}{((G_m - G_o)^2 + (B_m - B_o)^2)} - R_o$$

$$X_x = \frac{B_o - B_m}{((G_m - G_o)^2 + (B_m - B_o)^2)} - X_o$$

Where,

$G_m + jB_m$ = measured admittance of DUT in siemens

$R_o + jX_o$ = measured jig 'shorted' in ohms.

$G_o + jB_o$ = measured jig 'open' in siemens

This error corrected S_{11} measurement, can easily be converted into $R+-jX$, hence any other desired impedance parameter, exactly as described in the December 1997 article.[9]

frequencies below the series resonant point – and perhaps to one octave above it – is described exactly by the common equivalent circuit shown earlier.[9]

Simple measurement of impedance magnitude suffices to demonstrate this behaviour. All makers' data books include similar impedance frequency plots, permitting easy comparisons of resonant frequency and impedance minima between capacitor styles, **Fig. 6.**

However at higher frequencies, this simple circuit does not equate with the observed behaviour of practical capacitors.

With increasing frequency, the capacitor may exhibit either a single higher frequency parallel resonance or multiple resonances – exactly as are found with a mismatched transmission line.[11] These characteristics will depend on the dielectric's behaviour and the electrode resistances.

This behaviour is clearly measurable with porcelain and high-Q ceramic multilayer chips. Consequently Dielectric Laboratories[6] – a specialist maker of very high frequency capacitors – provides the transmission line simulation program *CapCad* for use with its products ■

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