

Operation and uses for the 570/571 IC compandor chip

PART I

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THIS ARTICLE DIVERGES somewhat from past *Op Amps for Audio* columns, and is also a great deal more than one of the typical *Noteworthy and New* items. The reason for these differences will be evident as you begin to grasp the details of operation and working of a new and fascinating IC chip. The Signetics NE570 and NE571 are monolithic IC *compondors*, devices which can be used for the audio gain control functions of compression and expansion, as well as other gain-controlled functions.

Although designed primarily for telephone trunk line communications service applications, the 570 and 571 devices possess performance specifications and built-in flexibility sufficient for a host of high quality audio signal processing uses. This first article surveys what the 570 and 571 are, how and what they do, and how to apply them to audio uses. We think you'll agree this somewhat unusual amount of interest is warranted when you see what these devices, with relative ease, can do with audio signals, and we think you will quickly grasp their importance to audio in general. Before this article is complete, you will be able to build projects which have heretofore been simply impossible or impractical.

This article is by intent both tutorial and practical, and features many ready-to-use 570/571 circuits. Information on 570/571 availability is included at the end of the article.

Basic Operation

Fig.1 is a block diagram of the 570 and 571. Both the 570 and 571 units consist of the functional components shown, and are in fact derived from the same basic chip. The difference between the two devices lies in their specifications, the 570 being the prime of the two units, with lower inherent distortion performance. The 571 has more relaxed basic specifications, but may be trimmed with outboard components to a performance level equal or near that of the 570.

Thus, unless otherwise stated hereafter, all of the circuits shown may use either device, with the final choice being up to the user.

The 570 and 571 are dual devices, consisting of two sets of the functional signal blocks indicated. These are a ΔG cell (for variable gain, if you will), a full wave rectifier which controls the gain of the ΔG cell, and an output op amp stage connected as shown. An on-chip 1.8V bias reference voltage is included, which supplies bias voltage to both halves of the dual circuit. This reference voltage, along with the supply voltage and ground pins, are the only things common to the two "halves" of the circuit, with the remainder of the pin functions shown being duplicated, one set per side of the 16 pin layout.

The 570 and 571 operate from single power supply voltages in the range of +6 to +24V, with quite low power, typical current drain being only 3mA (both sections). The devices are therefore well suited to battery operation, for not only is the current drain low but internal regulation makes operation highly immune to supply voltage, in general.

The ΔG Cell

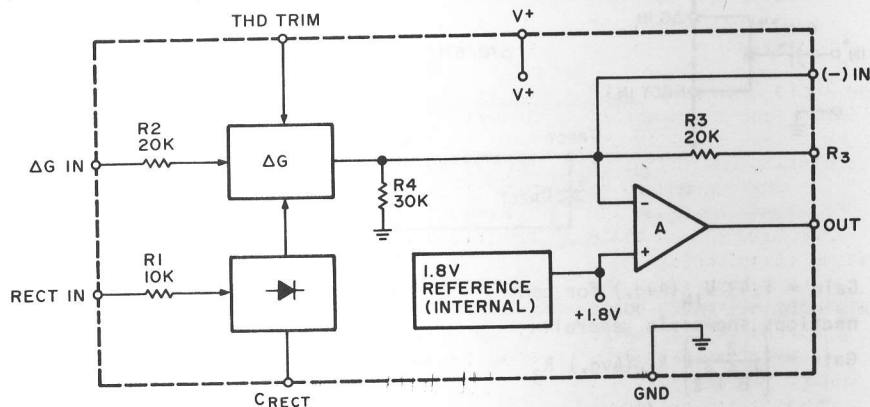
In operation the audio signal to be controlled is applied to the ΔG IN input through a coupling capacitor. AC coupling is necessary due to a +1.8V bias level present at the ΔG cell. The ΔG cell also constitutes

a virtual ground node, therefore the input impedance is simply the 20K value of R2, and the resulting input current will be $V_{in}/20K$. The ΔG cell is designed to accept a maximum of $\pm 100\mu A$ of input current ($200\mu A$ p-p), or a 1.4V max RMS sine wave level. Where necessary, higher input levels can be accommodated by including an external series resistor.

In its gain control mechanism, the net action of the ΔG cell in effect proportions the applied input current, and passes it on to the output op amp, where it is ultimately converted into the circuit's output voltage. The proportionality (or scaling factor) of the ΔG cell is in turn controlled by the rectifier, which produces an output current which directly controls the ΔG cell. The ΔG cell may be viewed as a current controlled, current scaling circuit. The controlling current is the DC output of the rectifier, and the controlled current is the audio signal. We haven't room here for the actual details of the ΔG cell circuit implementation, but they make interesting reading. Consult the references for further insight into the technique.

The ΔG cell, in short, compensates for natural transistor nonlinearities and temperature sensitivity, providing a stable and predictable programmable gain element with a dynamic control range of 100dB, with low signal distortion. The ultimate limitation on distortion is determined by the matching of the gain cells' internal transistor pairs, and this practical limit accounts for the aforementioned

Fig.1: 570, 571 Functional Diagram
(1 of 2 channels).



tioned differences between 570 and 571 devices. Solace arrives, however, in the news that either device can be trimmed using the THD TRIM terminal. When trimmed, typical devices can show THD figures of 0.1% or less (while untrimmed THD can be up to 0.5%). Distortion is this high, however, only at full scale audio signal inputs; at lower levels distortion drops rapidly, and noise becomes the limit to dynamic range.

Noise in a bipolar transistor transconductance multiplier such as is used here has been a topic of controversy in the audio fraternity, with many designers dismissing the technique as being practically useless because of its "inherently limited dynamic range," or because it is "inherently noisy." These objections are simply not justified when a linearized transconductance multiplier is implemented, as it is here. Signal to noise ratio in a 570 or 571 can be as high as 90dB in a 20kHz noise bandwidth, which of course easily exceeds almost all available program sources. Further, signal to noise improves (even beyond this figure) at lower working gains, where the circuit is most apt to be used.

Rectifier

The rectifier circuit of the 570/571 accepts a signal at the RECT IN terminal, and full wave rectifies this signal, converting it to a proportional DC signal which is used to control the AG cell. Like the AG IN input, the RECT IN input is biased at +1.8V and is AC coupled in normal operation. Input impedance is the value of R₁, or 10K. Full scale rectifier input current is 200μA peak, equivalent to 1.4V RMS into 10K.

After full wave rectification within the circuit, an external capacitor attached to the CRECT

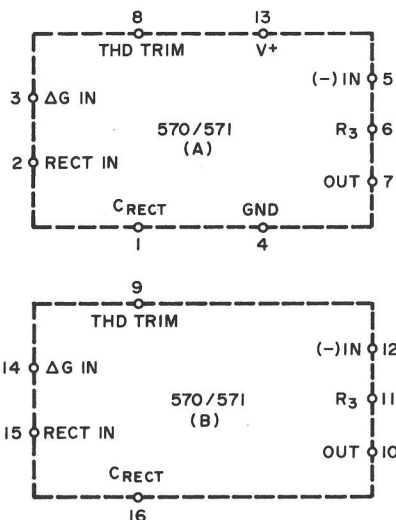


Fig. 2: 570, 571 Device symbol diagram and pinout.

terminal filters the DC signal, which is now equal to the average AC input level. The current fed to the ΔG cell as a gain control signal is then the average of the input AC signal.

Output Circuit

The output op amp used in the 570/571 is similar to a 741, and like the rest of the circuit is biased for minimum quiescent power drain. This amplifier can be used only in the inverting mode, and is set up for operation by connection of R₃, either as an input or feedback resistor. You may also use external resistors, as access is provided to the (-) input. The op amp is biased at its inputs to a DC level of +1.8V; connection of R₃ as a feedback resistor biases the output to 3V, optimum for a 6V supply level. You can achieve output biasing to other DC levels for greater swing by using external resistors in se-

ries or shunt combinations.

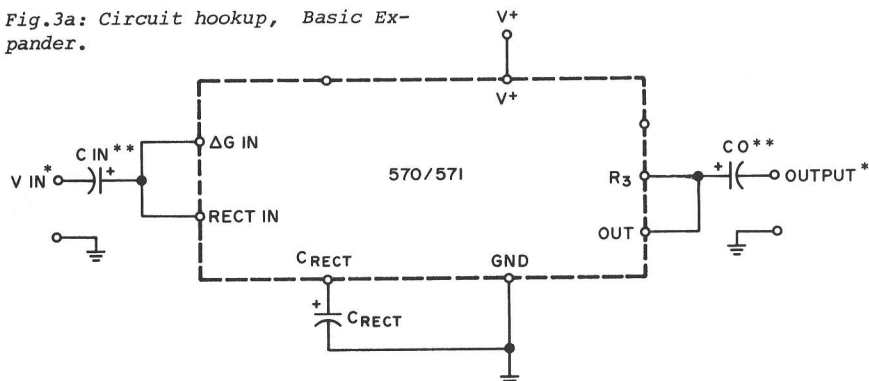
We gain further insight into the manner of 570/571's working by examining the two basic connections, as an expander and as a compressor. The subsequent schematic representations follow the device symbol diagram of Fig. 2, which also shows the pinout. Although it is not obvious from this drawing, the 570/571 is laid out in a symmetrical pattern (with the exception of supply pins), which facilitates PC layout.

Basic Expander

Connection and operation of a 570 or 571 as an expander is shown in Fig. 3. The hookup is shown in general form in Fig. 3a. The signal is applied in common to the ΔG IN and RECT IN terminals, through a common coupling capacitor, C_{IN}. An averaging capacitor, C_{RECT}, is connected from the C_{RECT} terminal to ground. The output is jumpered for use of R₃ as a feedback resistor. C_{IN} and C_O are input and output coupling capacitors, chosen for the desired circuit low end frequency response; they will typically be on the order of several microfarads for wide range audio work. (Note: observe correct polarity when using electrolytics.)

The gain of this circuit is described mathematically as $1.43 V_{IN}$, where V_{IN} is the average input

Fig. 3a: Circuit hookup, Basic Expander.



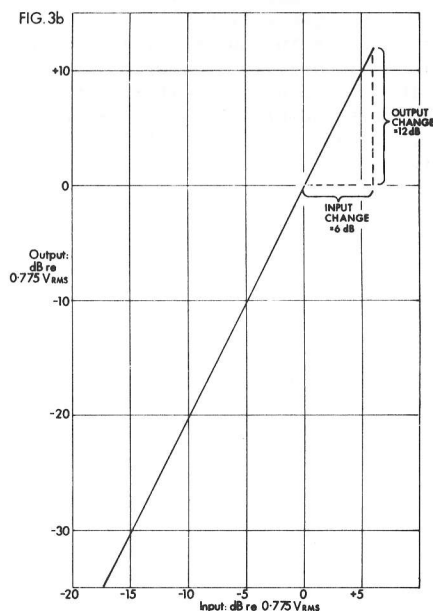
* Gain = $1.43 V_{IN}$ (Avg.) for connections shown--in general:

$$\text{Gain} = \left(\frac{2}{1 + R_1 R_2} \right) V_{IN} (\text{Avg.}) R_3$$

$I_B = 140\mu A$

$R_1 = 10K, R_2 = 20K, R_3 = 20K$

** Select C_{IN}, C_O for desired input/output corner freq.



voltage. The 570/571 circuit values are set up in such a way that the gain of this expander circuit is unity at an input level of 0.775 V (RMS) (or 0.7V (AVG)), a level obviously convenient for communications work. In the input/output graph of Fig.3b, you will note that indeed the output is 0.775V when the input is 0.775V.

The expansion ratio of this circuit is 1/2, thus an input change of 6dB will yield an output change of 12dB, which can be noted from the curve. Although this is a somewhat simplistic curve intended to illustrate the effect, it is true in practice that a 570/571 circuit will follow this relationship over an input dynamic range of 40dB or more (or 80dB or more of output range).

Errors which do occur at the low end of the dynamic range are largely due to the rectifier, and can be minimized. You may use separate coupling capacitors into the ΔG and RECT IN inputs to eliminate offset errors here, and a trim technique can be applied to the RECT IN terminal to optimize low level tracking (to be discussed below).

For the innovative designers out there, we include the circuit's pertinent complete design equations. You can shift the unity crossover point by alteration of R3. Or you may also adjust the effective value of R1 (or R2) by using series resistors at these terminals. I_B is an internal circuit constant, and is not alterable.

Basic Compressor

Fig.4 is a basic 570/571 compressor. Fig.4a details the circuit hookup, and 4b shows the input-output relation. You will note that this is the exact complement to the expander curve of 3b, as the addition of the two curves will yield a linear input-output curve.

The compressor circuit is somewhat more complex than the expander, because it requires some additional bias components. In this

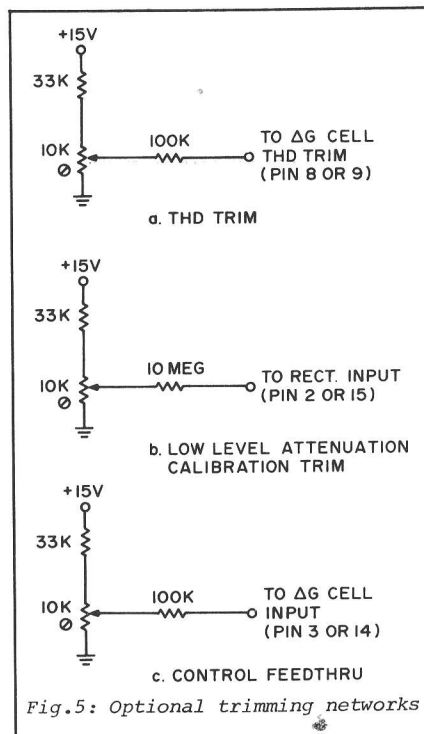
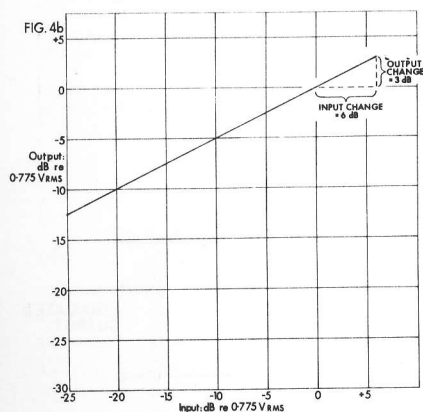


Fig.5: Optional trimming networks

circuit the ΔG cell is the AC feedback path, and a separate DC output bias path is provided by the R_{DC} resistors. These resistors bias the output up to a stable DC point, and C_{DC} removes any AC feedback. R_{DC} can typically be in the range of 20 to 30K, while C_{DC} is on the order 10 μ F.

C_F is a coupling capacitor to the ΔG and RECT IN inputs, while C_{IN} and C_O are input and output coupling capacitors (typically chosen as described previously).

You may have already intuitively noted that this circuit reduces gain for increasing input levels, as more signal feedback to the rectifier increases the ΔG cell current, which reduces gain by being in the feedback path.

Again, both the simple and general forms of design equations are shown. Unity gain crossover point in this circuit is also 0.775V, to complement the expander. The output

will change only 3dB for a 6dB input change, which is a 2/1 compression ratio. Modification of the unity gain crossover point (when desired) may be accomplished by using an external resistor in place of R3, connected to the (-) IN terminal.

This circuit can also be optimized for low level tracking, by using separate capacitors to the ΔG and RECT IN inputs, as in the compressor. Also you may trim as described in the next section.

Trimming Techniques

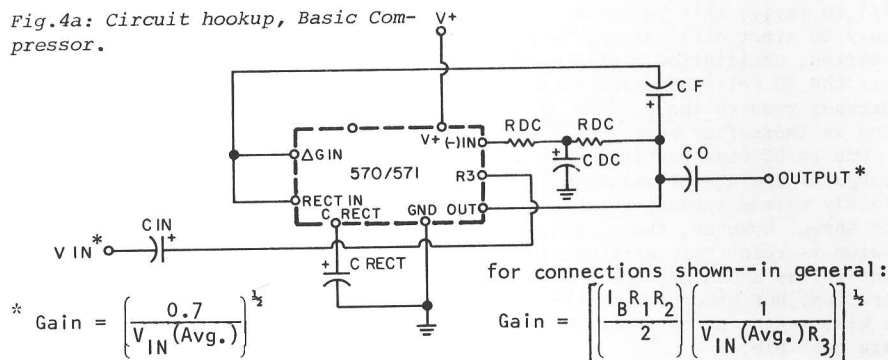
You may apply several trimming techniques to various 570/571 terminals, to optimize or enhance operation of either device. All of the techniques discussed here, and shown in Fig.5, are optional, and need be applied only when you want the highest performance.

Fig.5a shows the most useful of the three techniques, a trim for minimum THD. This circuit corrects for the offset voltage in the ΔG cell, in so doing minimizing its output second harmonic distortion content. It is quite effective, and in some cases can reduce distortion by as much as a factor of ten. The trimmer is adjusted for minimum output THD with the ΔG input driven to its maximum level.

The circuit of Fig.5b is useful in compensating for the bias current of the rectifier, which is typically 50-100nA. This DC bias current places a lower limit on tracking range, as it appears as an equivalent AC input, if uncorrected. The trimmer is adjusted for correct rectifier tracking, with an input 50-60dB below full scale. Note that this trim will not be effective unless a separate coupling capacitor is used at the rectifier input, as mentioned above.

The Fig.5c circuit can be used to minimize feedthrough of a gain change signal to the output. Ideally gain change signals should not be seen in the output, but if input signal levels are very low they may be noticeable. The trimmer is adjusted for minimum shift in the

Fig.4a: Circuit hookup, Basic Compressor.



output as gain is varied, with no AC signal applied to the ΔG cell.

Applications

We are now ready to discuss more specific circuit uses for the 570/571. All the circuits which follow are for single supply, +15V operation, but many can be battery operated if desired. A number of mixer type functions are included, thus the reader could readily use 570's or 571's to build a portable mixer with some interesting features.

Sine Wave Oscillator

Fig.6 shows how a 570/571 can be used to build a simple, self-AGC'd sine wave oscillator of the Wien type. This circuit is reasonably clean in terms of THD content and is suitable for a medium performance, fixed frequency sine wave source.

In this circuit, the Wien network is composed of components R1-C1 and C2-R2, which in conjunction with the output op amp of the 570/571 section A form the frequency determining filter. This filter resonates at a frequency of

$$f = \frac{1}{2\pi RC}$$

With equal element values as shown (R1 = R2 and C1 = C2) the networks' signal loss is 2/1 at the resonant frequency, and the phase relationship from the input at C1 to the output at R2-C8 is inverting. To sustain oscillation, a second gain stage must provide signal inversion for in-phase feedback, and a gain of 2. The gain must be held at 2 to sustain undistorted constant amplitude oscillations.

Section B of the 570/571 provides the required gain and phase inversion, in its output stage. By connecting the ΔG cell of this section as a compressor, the gain is automatically regulated to the required value to sustain undistorted oscillation. Resistors R3-R4 form the input resistance of the op amp gain network, and the chip's internal 20K resistor is used as the feedback resistor. Note that the initial nominal gain of this stage is higher than the required 2/1 (about 4/1 in fact); this factor is necessary to start oscillation. Once started, oscillations build up until the ΔG cell connected as a compressor reduces the gain to 2/1, and is thereafter self-sustaining.

Due to DC bias restrictions, the range of timing resistance has a fairly narrow spread, about 4 to 1 as shown. However, the capacitance value is relatively unrestricted. The values shown are for 400Hz operation, but other frequencies over a wide range, up to about 20kHz, are possible.

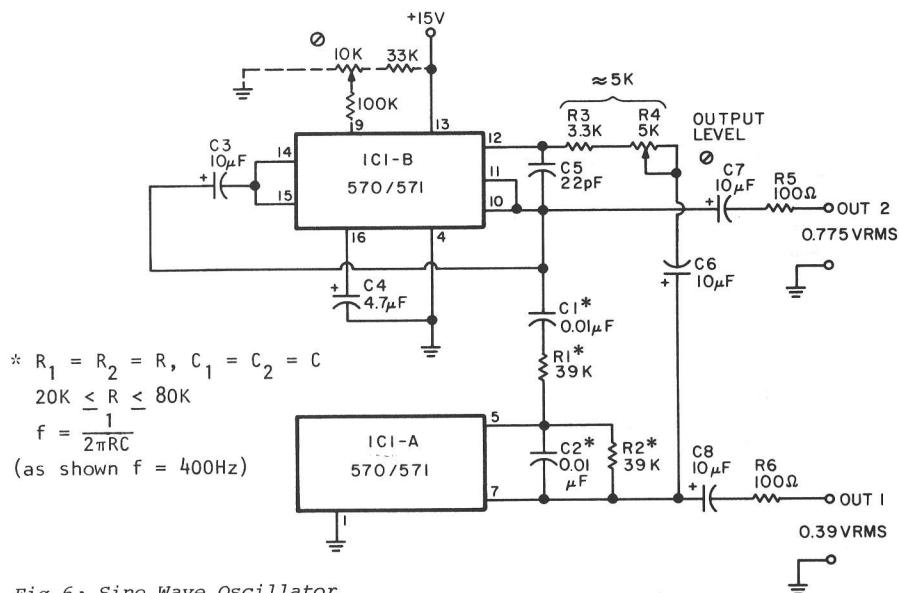


Fig.6: Sine Wave Oscillator

Distortion is reasonably low, but can vary due to two factors. If a 570 unit is used it will yield distortion of about 0.25%, without trimming. A 571 can also be used, and the optional trim network shown can reduce distortion at both outputs to about 0.1% or less. The ultimate level of distortion (for either device) is dependent upon the value of C4. Unfortunately, however, C4 cannot be increased indefinitely to decrease distortion, as it will lengthen settling time and thus compromise stability. For frequencies greatly removed from the example shown, C4's value should be optimized, going lower for higher frequencies, higher for lower frequencies.

Output amplitude is set by trim of the R3-R4 resistance, which accommodates variations in the 570/571 internal resistance. Output 2 can be adjusted in the range of 0.5 to 1V RMS, and output 1 will follow at half the output 2 level. Distortion is lowest at output 1, due to the filtering of the Wien network. Either or both outputs may be used, and they are well buffered against loading effects. If exact output levels are not desired, R3-R4 can

be replaced by a single resistor of 5k.

Amplitude Modulator

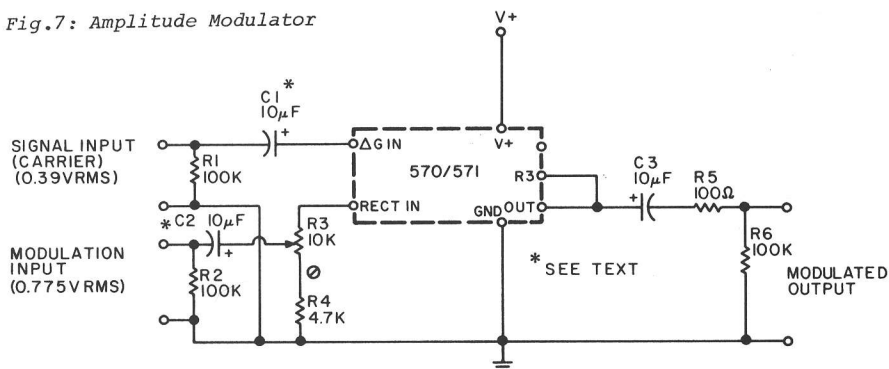
With the wide dynamic range gain control capability of the ΔG cell, various modulation schemes are possible using the 570/571. One of these is an amplitude modulator, shown in Fig.7.

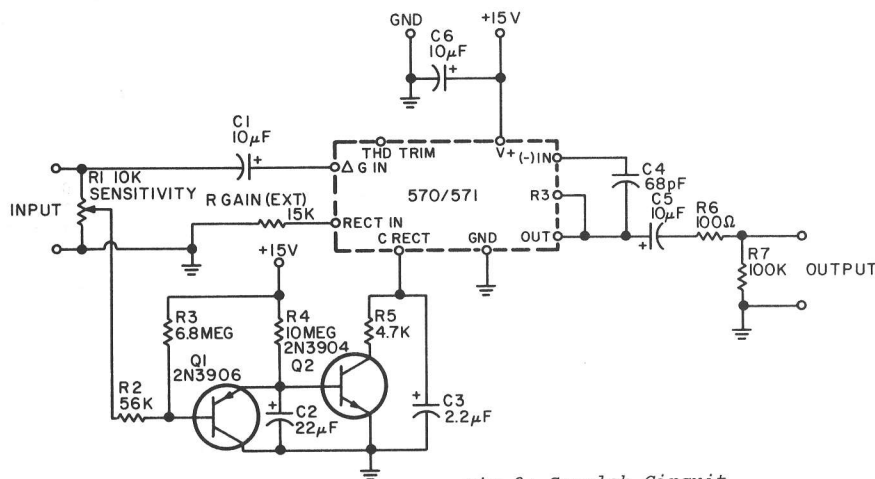
AM modulation requires a circuit which can vary the amplitude of a signal (the carrier) between 0 and 100% in a linear fashion. In this circuit, the ΔG cell of the 570/571 modulates the gain of the signal (carrier) channel, up to 100%.

With no modulating signal applied, the gain of the circuit is a nominal unity, as set up by the resistance R3 + R4 from RECT IN to ground. This resistance biases the ΔG cell to a mid-gain point. With modulation applied, negative modulation peaks double the gain, accomplishing 100% modulation. The resistance R3 is made variable, to accommodate modulating signals between 0.5 and 1V RMS in amplitude.

The circuit can be used as a modulation effects or tremolo generator. For very low modulating fre-

Fig.7: Amplitude Modulator





quencies such as below 10Hz, C2 should be increased to about 50μF. C1 is 10μF for wide band audio, but can be reduced for carrier frequencies above 100Hz. Both inputs are compatible with the 570/571 sine wave oscillator outputs, as shown here.

Squelch Circuit

Fig.8 operates as a gated amplifier controlled by the signal level or squelch. In this application, the 570/571 functions as a fixed gain stage when on. Signal level sensing and on/off control are performed by transistors Q1-Q2.

In the Q1-Q2 rectifier circuit PNP Q1 is a combination emitter follower and half wave rectifier. Q1 buffers the input signal as selected by sensitivity control R1, and discharges C2 on the negative peaks. Q1 can discharge C2 quickly, but C2 must recharge through R4.

With no signal applied, resistor R4 provides base drive for Q2 which causes it to saturate, clamping the C_{RECT} terminal to ground. This reduces the 570/571 gain to -80dB (or less). When an input signal is applied which overcomes the threshold bias set up by R2-R3 at the base of Q1, C2 is discharged, turning off Q2 and gating the amplifier on by releasing the clamp on C3.

Switching action is smooth, due to controlled transition times. A relatively long time constant is provided for by R4-C2. This time constant provides a delay prior to turnoff, which prevents premature switchoff between sentences, or other natural pauses.

Threshold sensitivity is a maximum of 200mV RMS with R1 fully advanced, and can of course be reduced as R1 is lowered. As shown, the on state gain is unity, as set

by $R_{\text{GAIN}}(\text{ext})$. This can be modified for higher gains, up to 8dB with $R_{\text{GAIN}}(\text{ext}) = 0$.

Mixer-Fader

The Fig.9 circuit shows how a single 570/571 device can be used as a logic level controlled mixer-fader amplifier. This circuit uses the two halves of the device as gated amplifiers, with a common output which is mixed in the output op amp of section A.

For either the A or B portion of the circuit, the 570/571 ΔG cells perform as controlled gated amplifiers, which are controlled by the drive applied to the respective RECT inputs, pins 2 or 15. For the A section, CMOS inverter stage IC2-4 gates the 570/571 ΔG cell on with a HIGH control input level. This provides a DC path to ground, the 15K gain programming resistor, R2. With an ON condition in the A channel, the A signal input is passed to the output with a nominal unity gain (as determined by R2).

When the control input is low, the conduction path through R2 is broken and the A channel ΔG cell switches off. The A channel gain goes smoothly to 0, as controlled by a time constant of $(10K)C2$.

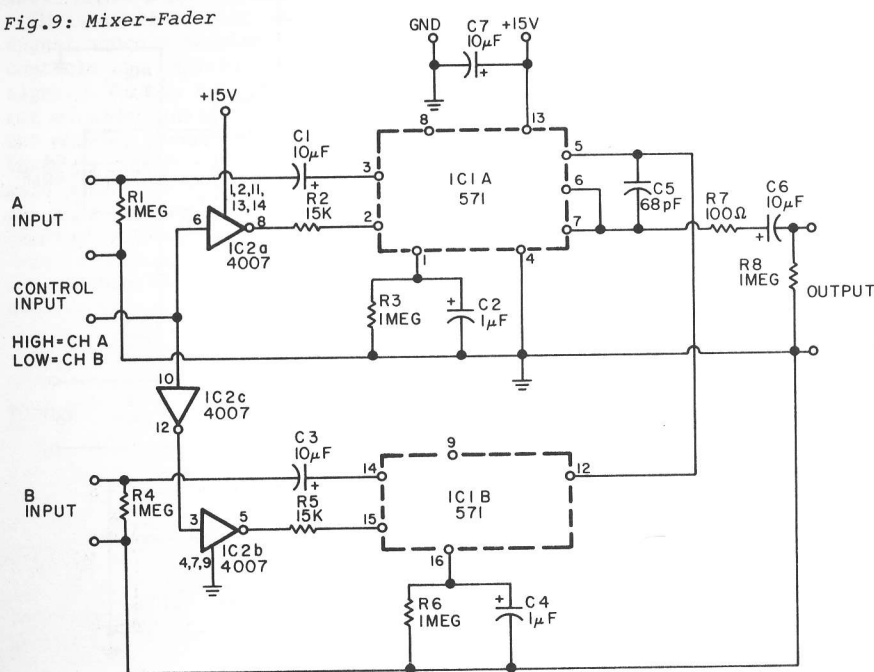
At the same time as the A channel logic inverter goes high, inverter IC2-b goes low, which programs the B channel to an ON condition, with the B channel's ΔG cell operating in a similar way to the A channel. The output of this ΔG cell (pin 12) is tied into the A section's amplifier summing input, at pin 5. With the B channel ΔG cell on, the B channel signal is passed to the output at unity gain (as determined by R5).

In the transition from off to on the B channel time constant is set by (10K)C4. Thus while channel A is going to zero gain, the opposite side, channel B is going to maximum gain. There is an overlapping transition period where both signals are on, due to time constants of the rectifier network. The effect is a "soft lap" type switching, very smooth and pleasant to the ear. You may vary transition time if you like, by adjusting C2 and C4 values.

This circuit can also be modified for gated mixing by separating the A and B channel control lines. Either or both may be ON as desired, in any combination. Adjust signal gains of each respective channel via R2 or R5.

Voltage Controlled Fader

An interesting and useful form of gain controlled circuit is an am-



With the values as shown, the circuit has 0dB of gain with a +3V control voltage, and a control sensitivity of 46mV/dB. Gain is -60dB @ +231V of input, the limit of useful working range. For further reductions of input voltage, the circuit switches to an OFF stage below about -62dB, where attenuation is more than 80dB. Within the 60dB working range tracking accuracy is within about 1dB of an ideal exponential law.

The circuit can be built up in a dual format with only four IC's: one 570 or 571, one 324 quad op amp, and two 3046 IC arrays. It may be used as either a dual channel unit, or strapped for stereo by tying the Vc inputs together.

Quest Electronics, PO Box 4430,
Santa Clara CA 95054 Prices:
NE570B: \$5.00 ea.; NE571B: \$5. ea
concluded on page 13

The diagram shows a 3V voltage regulator circuit. A +15V supply is connected to the IN pin of the LM317H or LM317P regulator. The ADJ pin is connected to a 0.1μF capacitor, which is also connected to the 3V output. The OUT pin is connected to a resistor R1 (100Ω), which is in series with resistor R2 (200Ω). The other end of R2 is connected to ground. The output voltage is 3V.

* NATIONAL SEMICONDUCTOR

LM317H *
OR
LM317P

IN

OUT

ADJ

R1 100Ω

R2 200Ω

0.1μF

ADJUST FOR 3.00V OUT

3 VOLT SOURCE

+ 3V
-

Fig.10: Voltage Controlled Fader

INPUT 0.775 VRMS

R1 1MEG

R2 10K

C1 10 μ F

R3 150K

R4 100K 0 GAIN CAL

R5 470K

R6 33K

R7 10K

R8 10MEG

R9 14.4K (SEE TEXT)

R10 1K

R11 1K

R12 8.2K

R13 22K

R14 100 Ω

R15 100K

R16 18K

R17 10 Ω

R18 1K

R19 1K

C2 0.1 μ F

C3 0.1 μ F

C4 68pF

C5 10 μ F

Q1* Q2* Q3* Q4* Q5*

IC1A(B) 570/571

IC2a(c) 324

IC2b(d) 324

DI IN914

LED1 MV5020 CHANNEL ACTIVE

V CONTROL VOLTAGE 46mV/dB 3V= 0dB 0.231V=-60dB

* P0 3046 IC TRANSISTOR ARRAY

+15V

-60 GAIN CAL

THD TRIM (9)

THD TRIM (8)

THD TRIM (10)

THD TRIM (11)

THD TRIM (12)

THD TRIM (13)

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THD TRIM (15)

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